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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,475	01/21/2004	Yoshitaka Ueda	001681A	9800

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EXAMINER	
LUU, AN T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/760,475	UEDA ET AL.	
	Examiner	Art Unit	
	An T. Luu	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/745,990.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1-21-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 24-28 and 31-35 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-3, 8 and 9 of U.S. Patent No. 6,707,328, hereinafter "the 328". Although the conflicting claims are not identical, they are not patentably distinct from each other because each and every limitation in claims 24-28 and 31-35 of the instant application read on claims of the 328. For instance, claim 24 reads on claim 1 of the 328; claim 25 reads on claim 2 of the 328; claims 26-28 read on claim 3 of the 328; claim 31 reads on claim 8 of the 328; and claims 32-35 read on claim 9 of the 328.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 24-37 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 24, the limitation "*a second power supply wire to be connected to the predetermined source of electric potential formed on said semiconductor substrate* ***independently of said first power supply wire*** *and connected between said input terminal and said second circuit of each of said plurality of said logic circuits*" (emphasis added) appears to be incorrect and/or misdescriptive since "input terminal" receives one voltage, namely *externally supplied power supply voltage* and both power supply wires (i.e., first and second) are coupled to "input terminal" and "the predetermined source of electric potential". Consequently, it is

impossible to have independently potential on the first power supply wire with respect to the second power supply wire. Claim 31 has similar problem as that of claim 24.

In claim 25, lines 3-4, the limitation "receiving said high--potential side pad electrode" appears to be an error due to cut and paste since the limitation on lines 3-4 is clearer and more meaningful by not having this limitation.

Claims 26-30 and 32-37 are rejected for being dependent on the rejected claims.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 24-37, as best understood, are rejected under 35 U.S.C. 102(b) as being anticipated by the Bonneau et al reference (US Patent 4,988,893).

Bonneau discloses in figure 2A a semiconductor integrated device comprising a semiconductor substrate (col. 2, line 57-65); a plurality of logic circuits (M2,S2) formed on said semiconductor substrate and each including a first circuit I21 for inputting a clock signal DO and a second circuit (I22 and I23) operating in synchronization with said clock signal input by said first circuit; an input terminal formed on said semiconductor substrate and receiving an externally supplied power supply voltage Vdd; a first power supply wire (line between transistor P21 and Vdd) to be connected to a predetermined source of electric potential Vdd formed on said semiconductor substrate and connected between said input terminal and said first circuit of each

of said plurality of said logic circuits; and a second power supply wire (line between transistor P24 and Vdd) to be connected to the predetermined source of electric potential formed on said semiconductor substrate and connected between said input terminal and said second circuit of each of said plurality of said logic circuits as required by claims 24 and 25. It is noted that a wire connecting Vdd and P21 is independent from the wire connecting Vdd and P24 and said **externally** power supply voltage includes a high-potential side power supply voltage Vdd wherein Vdd is commonly higher than GND.

As to claim 26, figure 2A discloses a low-potential side pad electrode (GND terminal) formed on said semiconductor substrate and receiving an externally supplied low-potential side power supply voltage GND; and a low-potential side power supply wire (i.e., line connecting GND to N22 and/or N25) formed on said semiconductor substrate for supplying said low-potential side power supply voltage at said low-potential side pad electrode to said first circuit and said second circuit of each of said plurality of said logic circuits.

As to claim 27, the low potential side power supply wire includes a first low-potential side power supply wire (i.e., wire connecting GND and N22) for supplying said low-potential side power supply voltage at said low-potential side pad electrode to said first circuit of each of said plurality of said logic circuits, and a second low-potential side power supply wire (i.e., wire connecting GDN and N25) for supplying said low-potential side power supply voltage at said low-potential side pad electrode to said second circuit of each of said plurality of said logic circuits.

As to claim 28, said low-potential side pad electrode includes a first low-potential side pad electrode (GND connecting to N22) formed on said semiconductor substrate and receiving

said low-potential side power supply voltage and a second low-potential side pad electrode (GND connecting to N25) formed on said semiconductor substrate and receiving said low-potential side power supply voltage, said low-potential side power supply wire includes a first low-potential side power supply wire (GND to N22) for supplying said low-potential side power supply voltage at said first low-potential side pad electrode to said first circuit of each of said plurality of said logic circuits, and a second low-potential side power supply wire (GND to N25) for supplying said low-potential side power supply voltage at said second low-potential side pad electrode to said second circuit of each of said plurality of said logic circuits.

As to claim 29, figure 2A discloses the second circuit (I22and I23) being structure as a latch which is known as a holding circuit.

As to claim 30, the circuit shown in figure 2A comprises p- and n-type transistors which are known as basic cells of standard cell systems.

As to claims 31-37, the scopes of these claims are similar to that of claims 24-30. Therefore, they are rejected for the same reasons set forth above. It is noted that each terminal labeled Vdd is seen as separate input terminal. The same reasoning is also applicable to each terminal GND.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to An T. Luu whose telephone number is 571-272-1746. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

An T. Luu
8-18-05 ATL

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